Amendments to the Claims

The following listing of the claims will replace all prior versions, and listings of the claims in the application:

Listing of Claims

43. (New) A method for implementing a class of N×N compressors each serving a connection request to route m incoming signals, m≤N, and for enabling the service of any connection request in a nonblocking way on the condition that the connection request is compliant to certain constraints, where each compressor in the class has a set of connection states and has an array of N input ports with N distinct input addresses and an array of N output ports with N distinct output addresses wherein the m incoming signals arrive at m distinct ones of the input ports determining m active input addresses and are destined for corresponding m distinct ones of the output ports determining m active output addresses, the method for each of the compressors comprising:

configuring an N×N k-stage interconnection network comprises (i) k stages of nodes, (ii) an interstage exchange between any succeeding two of the k stages, (iii) an input exchange, and (iv) an output exchange, and each node is filled with a switch of N-1 or fewer input ports and output ports, and

routing the incoming signals from the m distinct input ports to the corresponding m distinct output ports by activating one of the connection states such that the activated one of the connection states accommodates the connection request subject to said certain constraints on the connection request, wherein said certain constraints on the connection request are that: (1) the m active output addresses are consecutive upon a rotation of the ordering of the N output addresses, and (2) the correspondence between the m active input addresses and the m active output addresses is order preserving after the rotation,

said class excluding (i) those having a switch constructed from the reverse banyan network of switching cells appended with the inverse shuffle exchange and (ii) those having a switch constructed from the reverse shuffle-exchange network of switching cells appended with

the inverse shuffle exchange.

44. (New) The method as recited in claim 43 wherein each switch is a compressor.

45. (New) The method as recited in claim 43 wherein k=2 such that: (1) said N×N k-stage switching network becomes a two-stage interconnection network composed of a first stage of nodes being the input nodes and a second stage of nodes being the output nodes, an interstage exchange, and an output exchange, corresponding to the interstage exchange, appended to the network, and (2) each switch is a compressor.

46. (New) The method as recited in claim 45 wherein the two-stage interconnection network is configured as a 2X interconnection network.

47. (New) The method as recited in claim 43 wherein said N×N k-stage switching network is configured as a recursive 2X interconnection network having nodes and wherein each switch is a compressor.

48. (New) The method as recited in claim 47 wherein each of the nodes is a cell and each cell is filled with a 2×2 compressor.

49. (New) The method as recited in claim 48 wherein said 2×2 compressor is a switching cell.

50. (New) The method as recited in claim 43 wherein said N×N k-stage switching network is configured as a recursive 2X interconnection network of cells with each cell filled with a 2×2 compressor.

51. (New) The method as recited in claim 50 wherein the 2×2 compressor is a switching cell.

52. (New) The method as recited in claim 43 wherein said N×N k-stage switching network is configured as a banyan-type network whose trace and guide are both monotonically decreasing and wherein each of the 2×2 nodes of the banyan-type network is filled with a 2×2 compressor.

53. (New) The method as recited in claims from 52 wherein the 2×2 compressor is a switching cell.

54. (New) The method as recited in claim 43 wherein said N×N k-stage switching network is configured as a recursive plain 2-stage interconnection network of cells appended with a swap exchange and wherein each cell of the network is filled with a 2×2 compressor.

55. (New) The method as recited in claim 54 wherein the 2×2 compressor is a switching cell.

56. (New) The method as recited in claim 43 wherein said N×N k-stage switching network is configured as a divide-and-conquer network of cells appended with a swap exchange and wherein each cell of the network is filled with a 2×2 compressor

57. (New) A class of N×N compressors each serving a connection request to route m incoming signals, m≤N, and for enabling the service of any connection request in a nonblocking way on the condition that the connection request is compliant to certain constraints, each of the compressors comprising:

an array of N input ports with N distinct input addresses and an array of N output ports with N distinct output addresses wherein the m incoming signals arrive at m distinct ones of the input ports determining m active input addresses and are destined for corresponding m distinct ones of the output ports determining m active output addresses,

an NxN k-stage switching network defined by a set of connection states comprising (i) k stages of nodes, (ii) an interstage exchange between any succeeding two of the k

stages, (iii) an input exchange and (iv) an output exchange, and wherein each node is filled with a switch having N-1 or fewer input ports and output ports, and

control circuitry, coupled to the switching network, for routing the incoming signals from the m distinct input ports to the corresponding m distinct output ports by activating one of the connection states such that the activated one of the connection states accommodates the connection request subject to said constraints on the connection request, wherein said constraints on the connection request are that: (1) the m active output addresses are consecutive upon a rotation of the ordering of the N output addresses, and (2) the correspondence between the m active input addresses and the m active output addresses is order preserving after the rotation,

said class excluding (i) those having a switch constructed from the reverse banyan network of switching cells appended with the inverse shuffle exchange and (ii) those having a switch constructed from the reverse shuffle-exchange network of switching cells appended with the inverse shuffle exchange.

58. (New) The compressor as recited in claim 57 wherein each switch is a compressor.

59. (New) The compressor as recited in claim 57 wherein k=2 such that: (1) said N×N k-stage switching network becomes a two-stage interconnection network comprising a first stage of nodes being the input nodes and a second stage of nodes being the output nodes, an interstage exchange, and an output exchange, corresponding to the interstage exchange, appended to the network, and (2) each switch is a compressor.